Data Sheet

SST 28SF040
5.0V-only 4 Megabit
SuperFlash EEPROM

June 1997

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5.0V-only 4 Megabit
SuperFlash EEPROM

Features:

Single 5.0-Volt Read and Write Operations
CMOS SuperFlash EEPROM Technology
- Endurance: 100,000 Cycles (typical)
- Greater than 100 years Data Retention

Memory Organization: 512K x 8
Sector Erase Capability: 256 bytes per Sector
Low Power Consumption:
- Active Current: 15 mA (typical)
- Standby Current: 5 µA (typical)

Fast Sector Erase/Byte Program Operation
- Byte Program Time: 35 µs (typical)
- Sector Erase Time: 2 ms (typical)
- Complete Memory Rewrite: 20 sec (typical)

Fast Access Time: 120, 150, and 200 ns
Latched Address and Data
Hardware and Software Data Protection
- 7-Read-Cycle-Sequence Software Data Protection

End of Write Detection
- Toggle Bit
- Data# Polling

TTL I/O Compatibility
Packages Available
- 40-Pin TSOP (10 mm x 20 mm)
- 32-Pin TSOP (8 mm x 20 mm)
- 32-Pin PLCC
- 32-Pin PDIP

Product Description

The 28SF040 is a 512K x 8 bit CMOS sector erase, byte program EEPROM. The 28SF040 is manufactured using SST's proprietary, high performance CMOS SuperFlash EEPROM Technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternative approaches. The 28SF040 erases and programs with a 5.0-volt only power supply. The 28SF040 conforms to JEDEC standard pinouts for byte wide memories and is compatible with existing industry standard EPROM, flash EPROM and EEPROM pinouts.

Featuring high performance programming, the 28SF040 typically byte programs in 35 µs. The 28SF040 typically sector erases in 2 ms. Both program and erase times can be optimized using interface features such as Toggle bit or Data# Polling to indicate the completion of the write cycle. To protect against an inadvertent write, the 28SF040 has on chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 28SF040 is offered with a guaranteed sector endurance of 10^4 and 10^3 cycles. Data retention is rated greater than 100 years.

The 28SF040 is best suited for applications that require reprogrammable nonvolatile mass storage of program, configuration, or data memory. For all system applications, the 28SF040 significantly improves performance and reliability, while lowering power consumption when compared with floppy diskettes or EPROM approaches. EEPROM technology makes possible convenient and economical updating of codes and control programs on-line. The 28SF040 improves flexibility, while lowering the cost of program and configuration storage application.

Figure 1 shows the functional blocks of the 28SF040. Figures 2A, 2B, and 3 show the pin assignments for the 40 pin TSOP, 32 pin TSOP, 32 pin PDIP, and 32 pin PLCC packages. Pin description and operation modes are described in Tables 1 through 4.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first. Note, during the software data protection sequence the address are latched on the rising edge of OE# or CE#, whichever occurs first.

Command Definitions

Table 3 contains a command list and a brief summary of the commands. The following is a detailed description of the operations initiated by each command.

Sector_Erase Operation

The Sector_Erase operation erases all bytes within a sector and is initiated by a setup command and an execute command. A sector contains 256 bytes. This sector erasability enhances the flexibility and usefulness of the 28SF040, since most applications only need to change a small number of bytes or sectors, not the entire chip.

The setup command is performed by writing 20H to the device. The execute command is performed by writing D0H to the device. The erase operation begins with the rising edge of the WE# or CE#, whichever occurs first and terminates automatically by using an internal timer. The end of Erase can be determined using either Data# Polling, Toggle Bit, or Successive Reads detection methods. See Figure 9 for timing waveforms.

The two-step sequence of setup command followed by an execute command ensures that only memory contents within the addressed sector are erased and other sectors are not inadvertently erased.

Sector_Erase Flowchart Description

Fast and reliable erasing of the memory contents within a sector is accomplished by following the sector erase flowchart as shown in Figure 18. The entire procedure consists of the execution of two commands. The Sector_Erase operation will terminate after a maximum of 4 ms. A Reset command can be executed to terminate the erase operation; however, if the erase operation is terminated prior to the 4 ms time-out, the sector may not be fully erased. An erase command can be reissued as many times as necessary to complete the erase operation. The 28SF040 cannot be “overerased”.

Chip_Erase Operation

The Chip_Erase operation is initiated by a setup command (30H) and an execute command (30H). The Chip_Erase operation allows the entire array of the 28SF040 to erase in one operation, as opposed to 2048 sector erase operations. Using the Chip_Erase operation will minimize the time to rewrite the entire memory array. The Chip_Erase operation will terminate after a maximum of 20 ms. A Reset command can be executed to terminate the erase operation; however, if the erase operation is terminated prior to the 20 ms time-out, the Chip may not be completely erased. If an erase error occurs an erase command can be reissued as many times as necessary to complete the erase operation. The 28SF040 cannot be “overerased”. (See Figure 8)

Byte_Program Operation

The Byte_Program operation is initiated by writing the setup command (10H). Once the program setup is performed, programming is executed by the next WE# pulse. See Figures 5 and 6 for timing waveforms. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first, and begins the program operation. The program operation is terminated automatically by an internal timer. See Figure 16 for the programming flowchart.

The two-step sequence of a setup command followed by an execute command ensures that only the addressed byte is programmed and other bytes are not inadvertently programmed.

The Byte_Program Flowchart Description

Programming data into the 28SF040 is accomplished by following the Byte_Program flowchart shown in Figure 16. The Byte_Program command sets up the byte for programming. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first and begins the program operation. The end of program can be detected using either the Data# Polling, Toggle bit, or Successive reads.

Reset Operation

The Reset command is provided as a means to safely abort the erase or program command sequences. Following either setup commands (erase or program) with a write of FFH will safely abort the operation. Memory contents will not be altered. After the Reset command, the device returns to the read mode. The Reset command does not enable software data protection. See Figure 7 for timing waveforms.

Read

The Read operation is initiated by setting CE#, and OE# to logic low and setting WE# to logic high (See Table 2). See Figure 4 for read memory timing waveform. The read operation from the host retrieves data from the array. The device remains enabled for read until another operation mode is accessed. During initial power-up, the device is in the read mode and is software data protected. The device must be unprotected to execute a write command.

The read operation of the 28SF040 is controlled by OE# and CE# at logic low. When CE # is high, the chip is deselected and only standby power will be consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when CE# and OE# are high.

Read_ID operation

The Read_ID operation is initiated by writing a single command (90H). A read of address 0000H will output the manufacturer's code (BFH). A read of address 0001H will output the device code (04H). Any other valid command will terminate this operation.

Data Protection

In order to protect the integrity of nonvolatile data storage, the 28SF040 provides both hardware and software features to prevent inadvertent writes to the device, for example, during system power-up or power-down. Such provisions are described below.

Hardware Data Protection

The 28SF040 is designed with hardware features to prevent inadvertent writes. This is done in the following ways:

1. Write Inhibit Mode: OE# low, CE#, or WE# high will inhibit the write operation.
2. Noise/Glitch Protection: A WE# pulse width of less than 15 ns will not initiate a write cycle.
3. V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5V.
4. After power-up the device is in the read mode and the device is in the software data protect state.

Software Data Protection (SDP)

The 28SF040 has software methods to further prevent inadvertent writes. In order to perform an erase or program operation, a two-step command sequence consisting of a set-up command followed by an execute command avoids inadvertent erasing and programming of the device.

The 28SF040 will default to software data protection after power up. A sequence of seven consecutive reads at specific addresses will unprotect the device The address sequence is 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH. The address bus is latched on the rising edge of OE# or CE#, whichever occurs first. A similar seven read sequence of 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 040AH will protect the device. Also refer to Figures 10 and 11 for the 7 read cycle sequence Software Data Protection. The I/O pins can be in any state (i.e., high, low, or tristate).

Write Operation Status Detection

The 28SF040 provides three means to detect the completion of a write cycle, in order to optimize the system write cycle time. The end of a write cycle (erase or program) can be detected by three means: 1) monitoring the Data# Polling bit; 2) monitoring the Toggle bit; or 3) by two successive read of the same data. These three detection mechanisms are described below.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with the DQ used. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

The 28SF040 features Data# Polling to indicate the write operation status. During a write operation, any attempt to read the last byte loaded during the byte-load cycle will receive the complement of the true data on DQ_7. Once the write cycle is completed, DQ_7 will show true data. The device is then ready for the

next operation. See Figure 12 for Data Polling timing waveforms. In order for Data# Polling to function correctly , the byte being polled must be erased prior to programming.

Toggle Bit (DQ_6)

An alternative means for determining the write operation status is by monitoring the Toggle Bit, DQ_6. During a write operation, consecutive attempts to read data from the device will result in DQ_6 toggling between logic 0 (low) and logic 1 (high). When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 13 for Toggle Bit timing waveforms.

Successive Reads

An Alternative means for determining an end of a write cycle is by reading the same address for two consecutive data matches.

Product Identification

The Product Identification mode identifies the device as 28SF040 and the manufacturer as SST. This mode may be accessed by hardware and software operations. The hardware operation is typically used by an external programmer to identify the correct algorithm for the 28SF040. Users may wish to use the software operation to identify the device (i.e., using the device code). For details see Table 2 for the hardware operation and Figure 19 for the software operation. The manufacturer and device codes are the same for both operations.

Product Identification Table

	Byte	Data
Manufacturer Code	0000 H	BF H
Device Code	0001 H	04 H

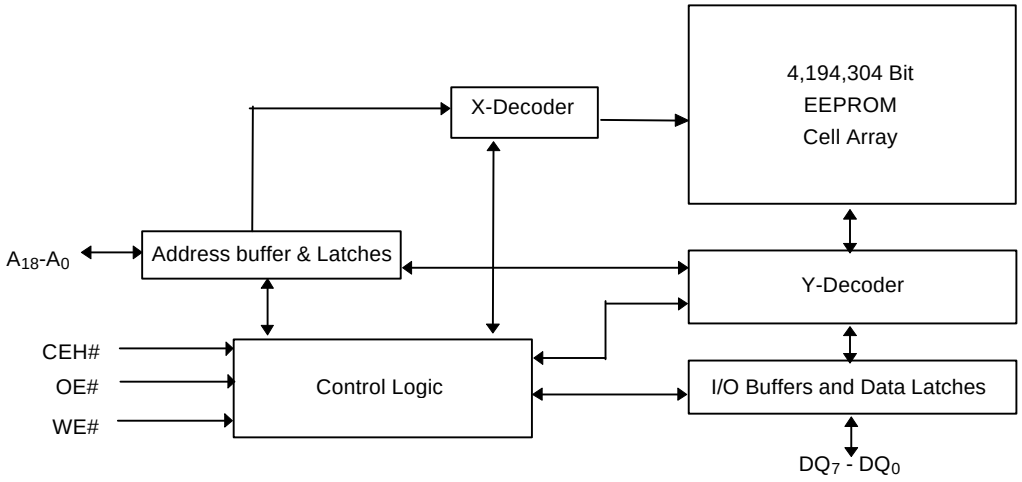


Figure 1: Functional Block Diagram of SST 28SF040

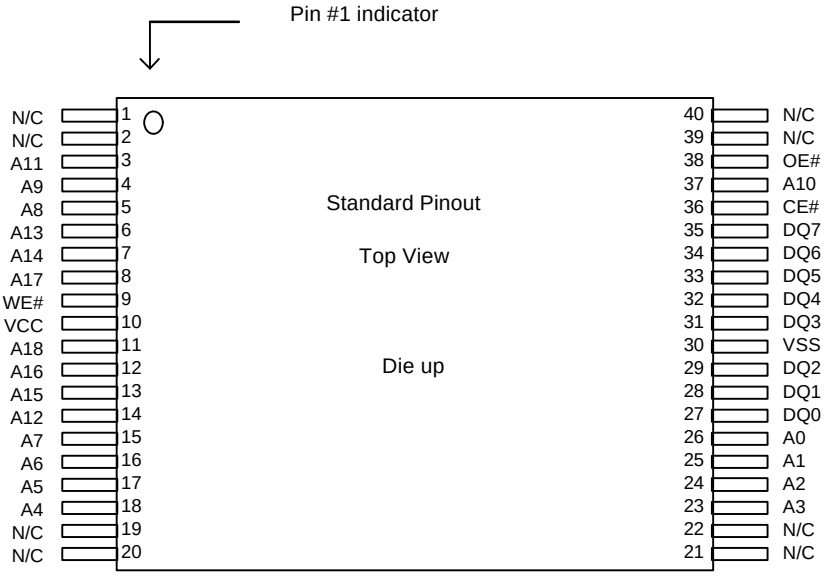


Figure 2A: Standard Pin Assignments for 40-pin TSOP Pac kages

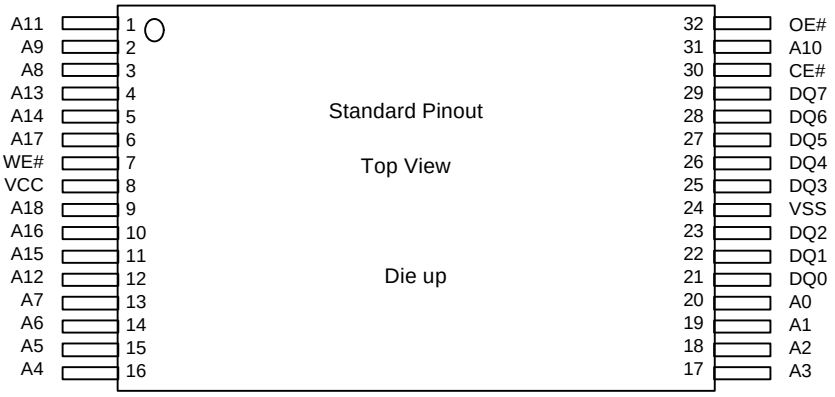


Figure 2B: Standard Pin Assignments for 32-pin TSOP Packages

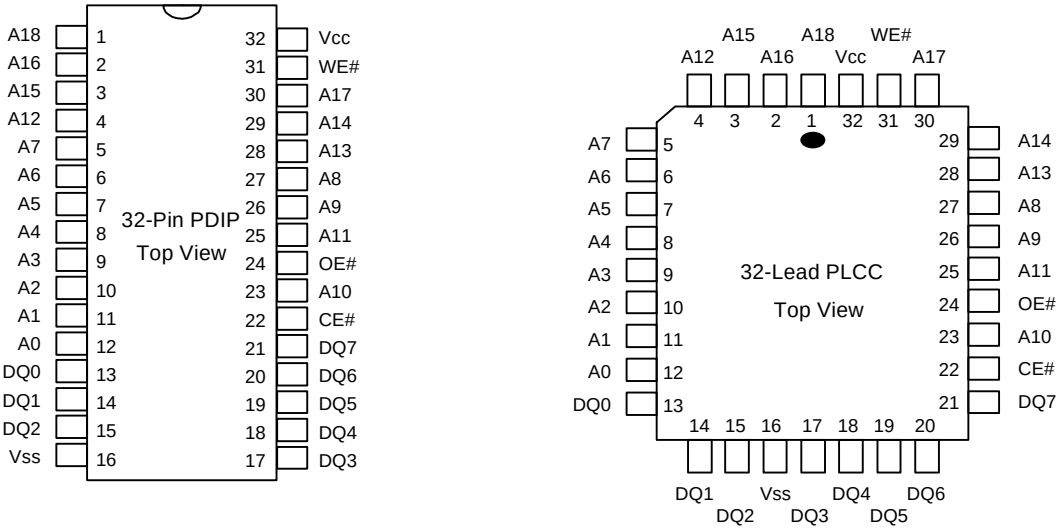


Figure 3: Pin Assignments for 32-pin Plastic DIPs and 32-pin PLCCs

Table 1: Pin Description

Symbol	Pin Name	Functions
A_{18}-A_8	Row Address Inputs	To provide memory addresses. Row addresses define a sector.
A_7-A_0	Column Address Inputs	Selects the byte within the sector.
DQ_7-DQ_0	Data Input/Output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE#, CE # is high.
CE#	Chip Enable	To activate the device when CE # is low.(1)
OE#	Output Enable	To gate the data output buffers.(1)
WE#	Write Enable	To control the write operations.(1)
Vcc	Power Supply	To provide 5-volt supply (± 10%)
Vss	Ground	

Note: (1) This pin is considered an input for the purposes of the DC Operation Characteristics Table.

Table 2: Operation Modes Selection

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Byte Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 3
Sector Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}, See Table 3
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Table 3
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IL}
				Device Code (04)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 3
SDP Enable & Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 3
Reset	V_{IL}	V_{IH}	V_{IL}		See Table 3

Table 3: Software Command Summary

Command Summary	Required Cycle(s)	Setup Command Cycle			Execute Command Cycle			SDP[5]
		Type[1]	Addr[2,3]	Data[4]	Type[1]	Addr[2,3]	Data[4]	
Sector_Erase	2	W	X	20H	W	SA	D0H	N
Byte_Program	2	W	X	10H	W	PA	PD	N
Chip_Erase	2	W	X	30H	W	X	30H	N
Reset	1	W	X	FFH				Y
Read_ID	3	W	X	90H	R	(8)	(8)	Y
Software_Data_Protect	7	R	(6)					
Software_Data_Unprotect	7	R	(7)					

Notes:

1. Type definition: W = Write, R = Read, X= don't care
2. Addr (Address) definition: SA = Sector Address = A_{18} - A_8, sector size = 256 bytes; A_7 - A_0 = X for this command.
3. Addr (Address) definition: PA = Program Address = A_{18} - A_0.
4. Data definition: PD = Program Data, H = number in hex.
5. SDP = Software Data Protect mode using 7 Read Cycle Sequence.
   a) Y = the operation can be executed with protection enabled
   b) N = the operation cannot be executed with protection enabled
6. Refer to Figure 11 for the 7 Read Cycle sequence for Software_Data_Protect.
7. Refer to Figure 10 for the 7 Read Cycle sequence for Software_Data_Unprotect.
8. Address 0000H retrieves the manufacturer' code of BFH and address 0001H retrieves the device code of 04H.

Table 4: Memory Array Detail

Sector Select	Byte Select
A_{18} - A_8	A_7 - A_0

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential	-0.5V to V_{CC} + 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential	-1.0V to V_{CC} + 1.0V
Voltage on A_9 Pin to Ground Potential	-0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C)	1.0W
Through Soldering Temperature (10 Seconds)	300°C
Surface Mount Lead Soldering Temperature (3 Seconds)	240°C
Output Short Circuit Current(1)	100 mA

Note: (1) Outputs shorted for no more than one second. No more than one output shorted at a time.

Table 5: Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	5V±10%
Industrial	-40 °C to +85 °C	5V±10%

Table 6: AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 14 and 15

Table 7: DC Operating Characteristics

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
I_{CC}	Power Supply Current				CE# = OE# = V_{IL}, WE# = V_{IH}, all I/Os open
	Read		25	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min. V_{CC} = V_{CC} Max
	Program and Erase		40	mA	CE# = WE# = V_{IL}, OE# = V_{IH} V_{CC} = V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		3	mA	CE# = OE# = WE# = V_{IH}, V_{CC} = V_{CC} Max
I_{SB2}	Standby V_{CC} Current (CMOS input)		20	µA	CE# = OE# = WE# = V_{CC} -0.3V, V_{CC} = V_{CC} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN} = GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 µA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE# = OE# = V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

Table 8: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$ [1]	Power-up to Read Operation	10	ms
$T_{PU-WRITE}$ [1]	Power-up to Write Operation	10	ms

Table 9: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$ [1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN} [1]	Input Capacitance	V_{IN} = 0v	6 pF

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 10: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1,000 & 10,000[2]	Cycles	MIL-STD-883, Method 1033
T_{DR} [1]	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM} [1]	ESD Susceptibility Human Body Model	1000	Volts	MIL-STD-883, Method 3015
V_{ZAP_MM} [1]	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I_{LTH} [1]	Latch Up	100	mA	JEDEC Standard 17

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2]See Ordering Information for desired type.

AC Characteristics

Table 11: Read Cycle Timing Parameters

IEEE Symbol	Industry Symbol	Parameter	28SF040-120		28SF040-150		28SF040-200		Units
			Min	Max	Min	Max	Min	Max	
tAVAV	T_{RC}	Read Cycle Time	120		150		200		ns
tAVQV	T_{AA}	Address Access Time		120		150		200	ns
tELQV	T_{CE}	Chip Enable Access Time		120		150		200	ns
tGLQV	T_{OE}	Output Enable Access Time		50		70		75	ns
tEHQZ	T_{CLZ}[(1)]	CE# Low to Active Output	0		0		0		ns
tGHQZ	T_{OLZ}[(1)]	OE# Low to Active Output	0		0		0		ns
tELQX	T_{CHZ}[(1)]	CE# High to High-Z Output		30		40		40	ns
tGLQX	T_{OHZ}[(1)]	OE# High to High-Z Output		30		40		40	ns
tAXQX	T_{OH}[(1)]	Output Hold from Address Change	0		0		0		ns

Table 12: Erase/Program Cycle Timing Parameters

IEEE Symbol	Industry Symbol	Parameter	Min	Max	Units
tAVA	T_{BP}	Byte Program Cycle Time		40	µs
tWLWH	T_{WP}	Write Pulse Width (WE#)	100		ns
tAVWL	T_{AS}	Address Setup Time	10		ns
tWLAX	T_{AH}	Address Hold Time	50		ns
tELWL	T_{CS}	CE# Setup Time	0		ns
tWHEX	T_{CH}	CE# Hold Time	0		ns
tGHWL	T_{OES}	OE# High Setup Time	10		ns
tWGL	T_{OEH}	OE# High Hold Time	10		ns
tWLEH	T_{CP}	Write Pulse Width (CE#)	100		ns
tDVWH	T_{DS}	Data Setup Time	50		ns
tWHDX	T_{DH}	Data Hold Time	10		ns
tWHWL2	T_{SE}	Sector Erase Cycle Time		4	ms
	T_{RST}[(1)]	Reset Command Recovery Time		4	µs
tWHWL3	T_{SCE}	Software Chip_Erase Cycle Time		20	ms
tEHEL	T_{CPH}	CE# High Pulse Width	50		ns
tWHWL1	T_{WPH}	WE# High Pulse Width	50		ns
	T_{PCP}[(1)]	Protect Chip Enable Pulse Width	10		ns
	T_{PCH}[(1)]	Protect Chip Enable High Time	10		ns
	T_{PAS}[(1)]	Protect Address Setup Time	0		ns
	T_{PAH}[(1)]	Protect Address Hold Time	50		ns

Note: [(1)]This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

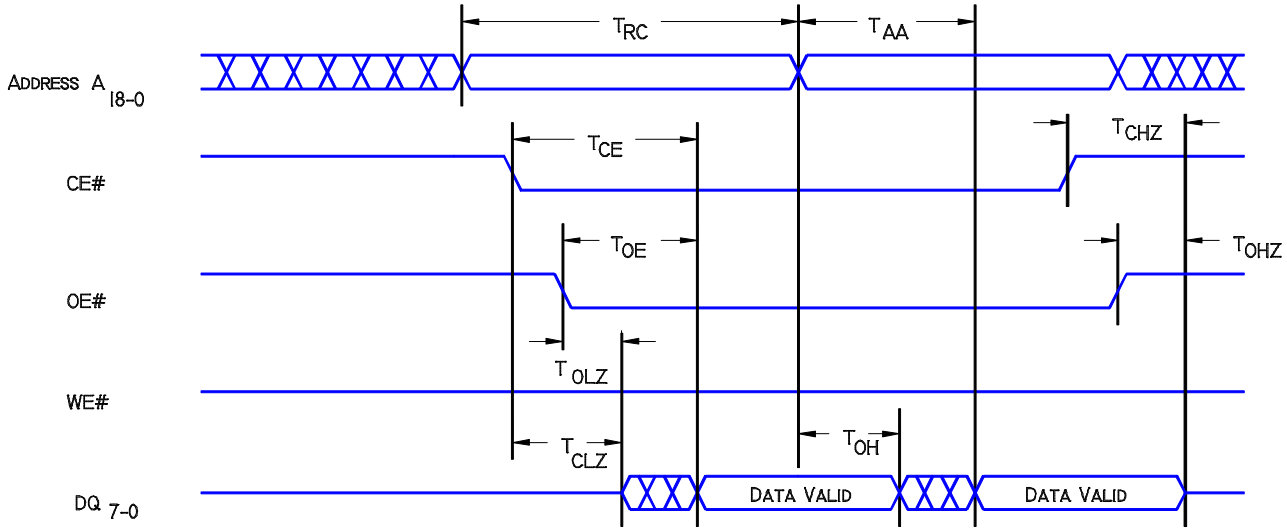


Figure 4: Read Cycle Timing Diagram

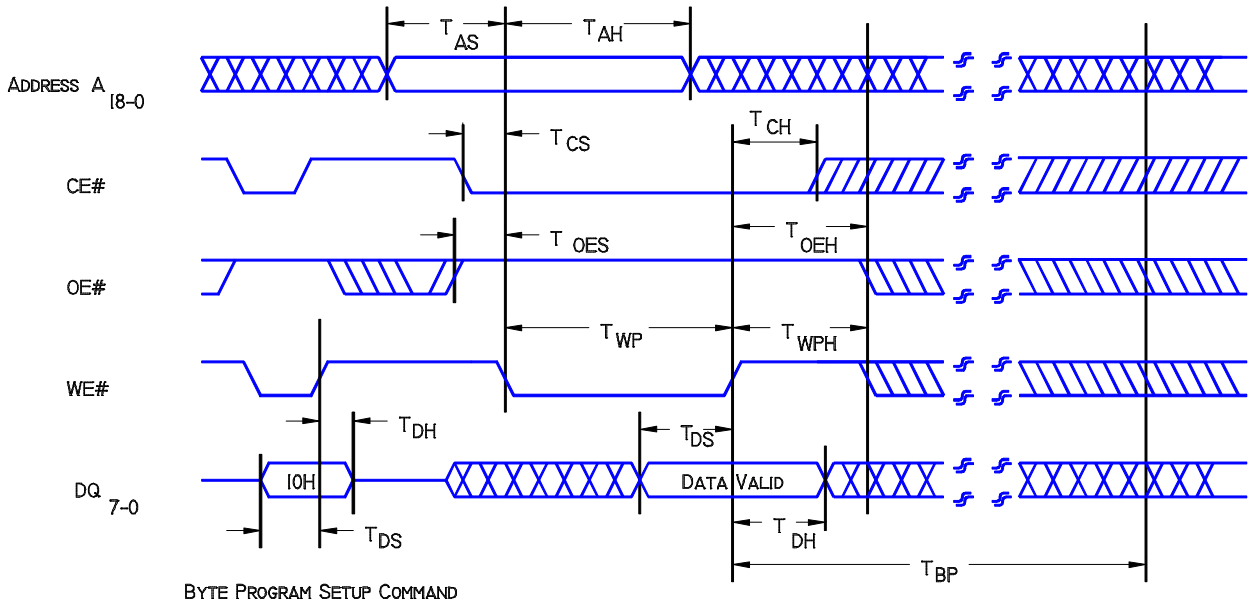


Figure 5: WE# Controlled Byte Program Timing Diagram

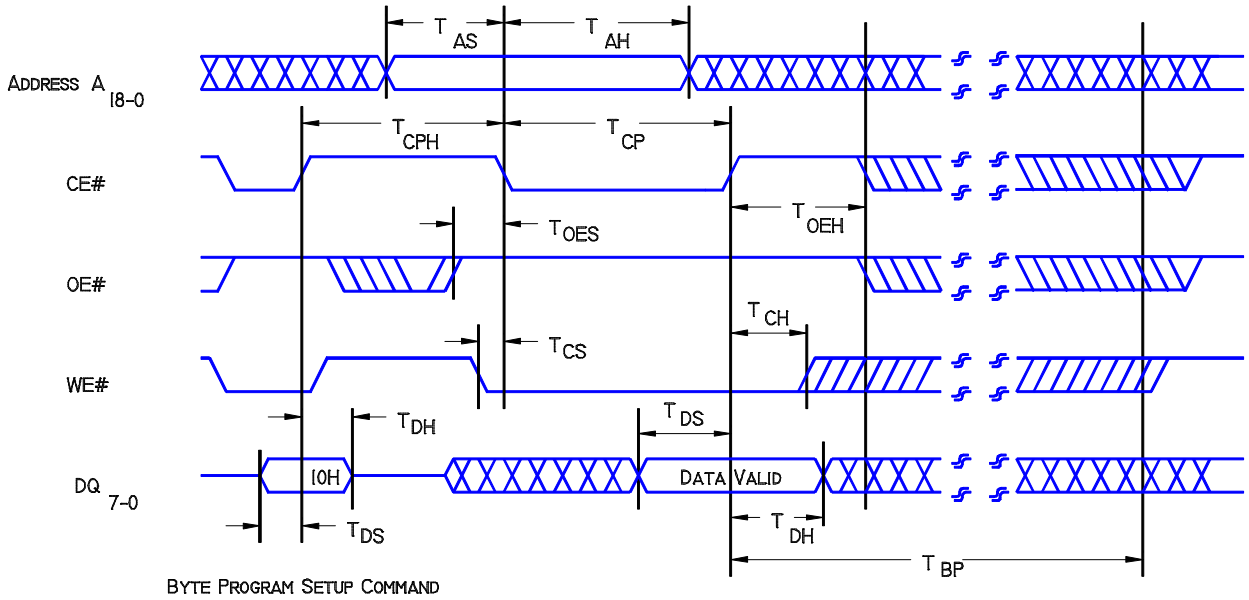


Figure 6: CE# Controlled Byte Program Timing Diagram

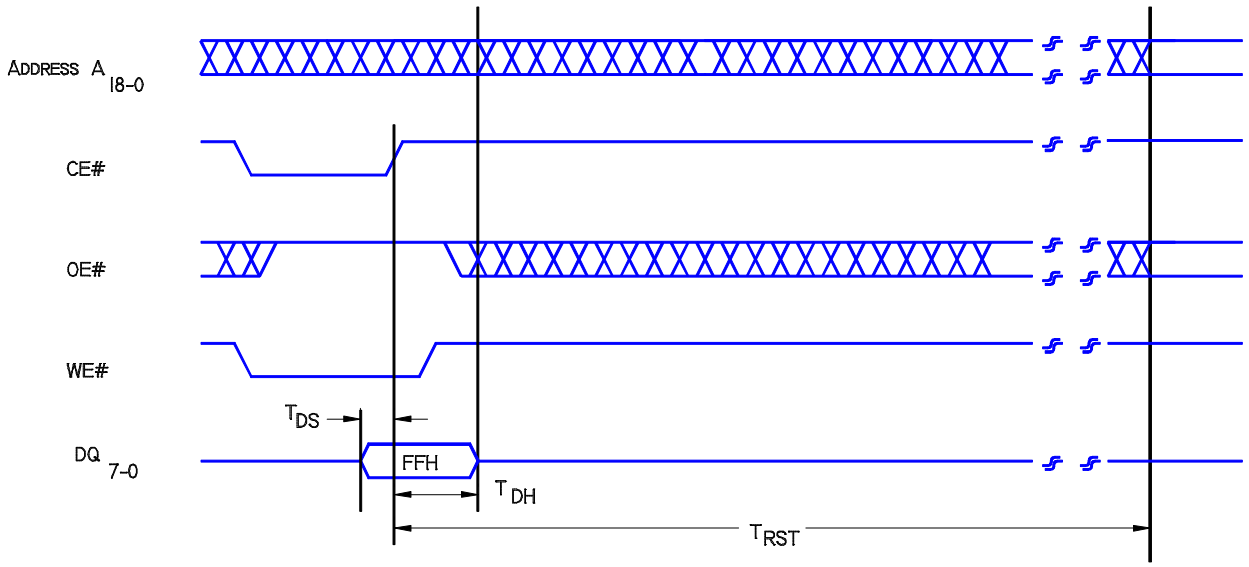


Figure 7: Reset Command Timing Dia gram

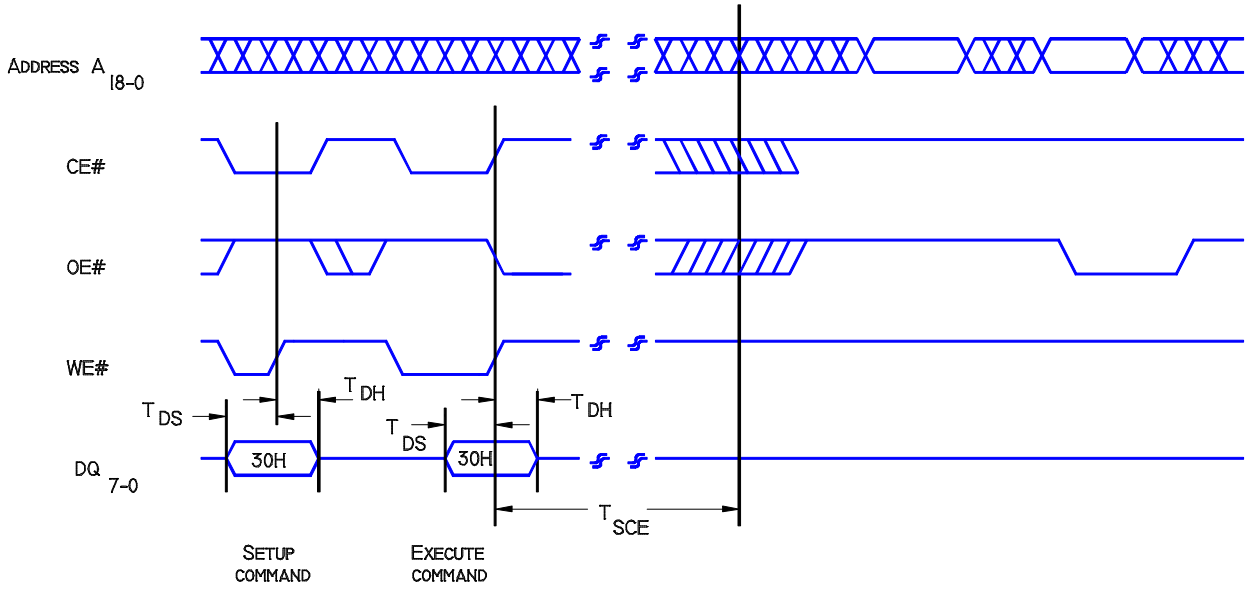


Figure 8: Chip_Erase Timing Diagram

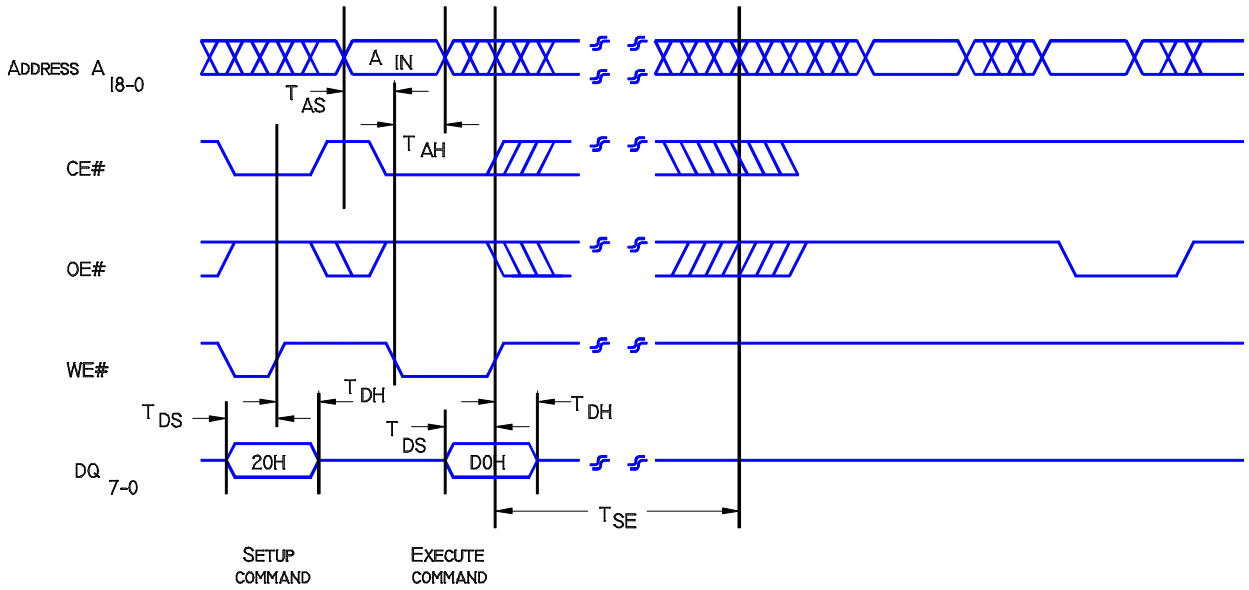
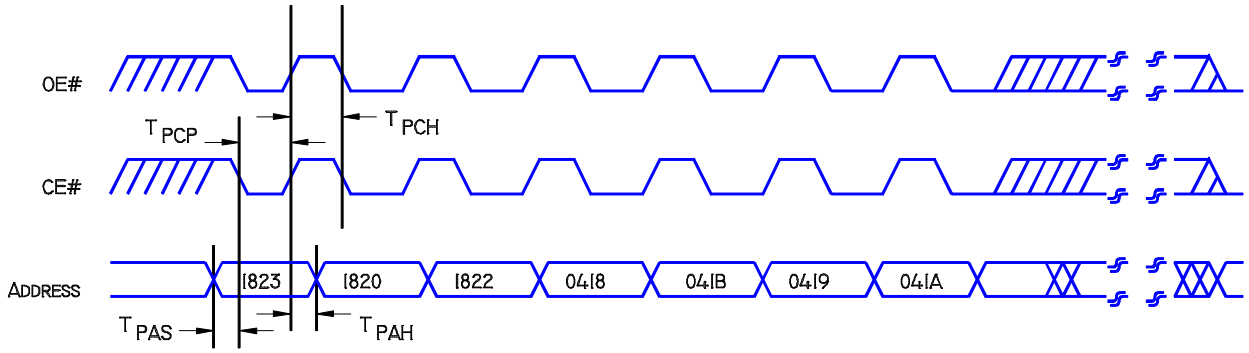


Figure 9: Sector Erase Timing Diagram



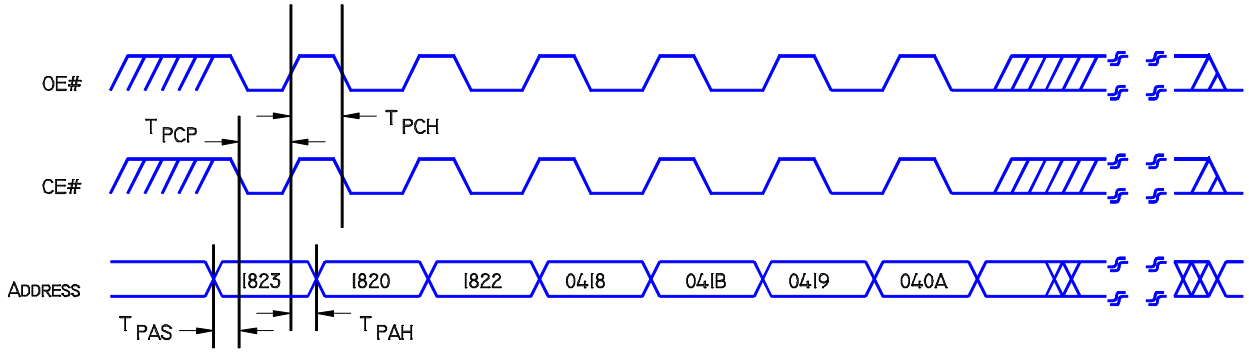
NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 10: Software Data Unprotect Timing Diagram



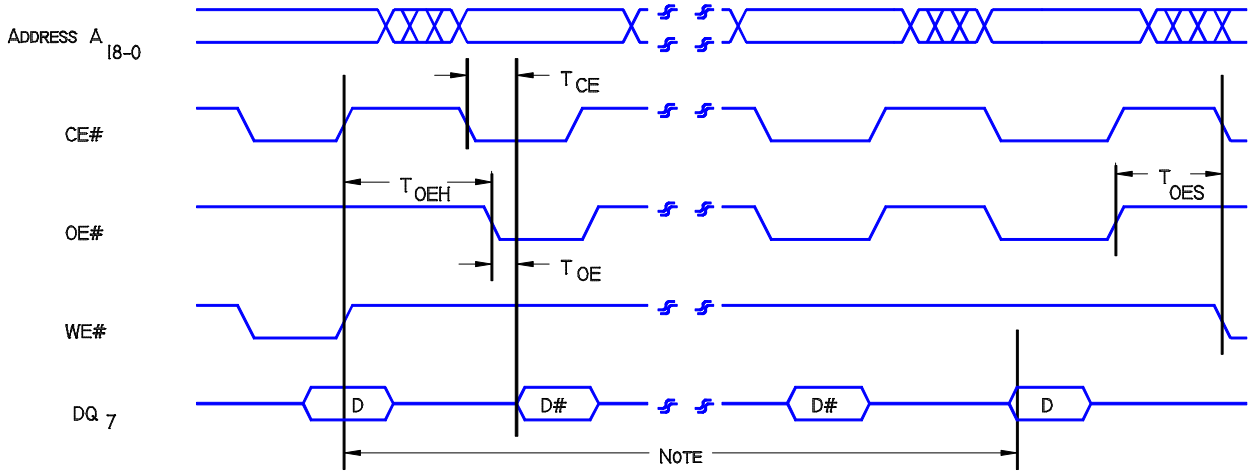
NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

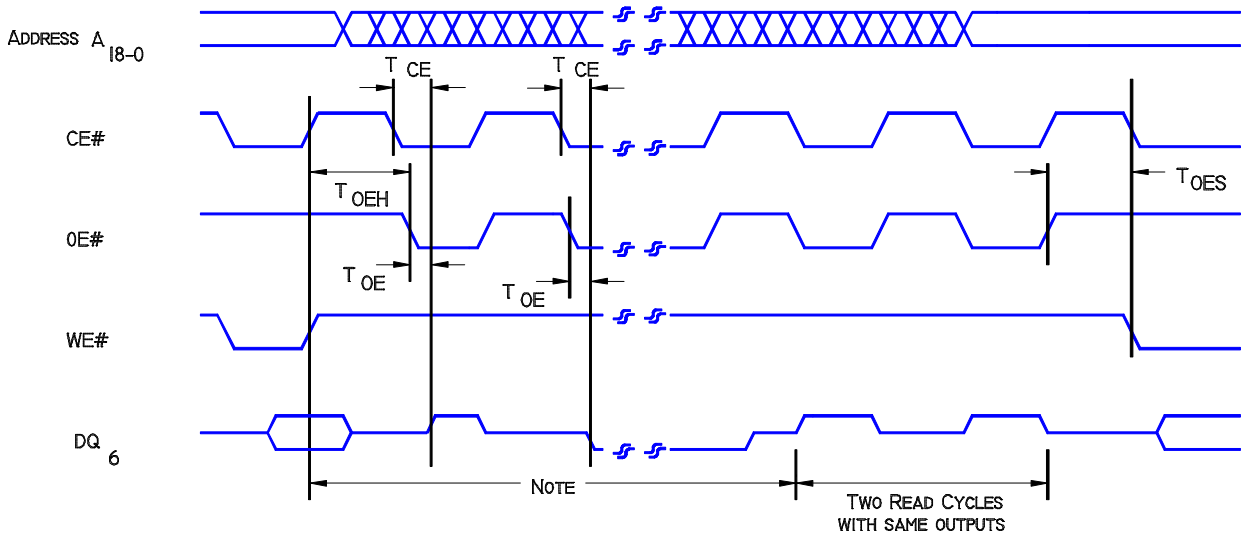
C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 11: Software Data Protect Timing Diagram



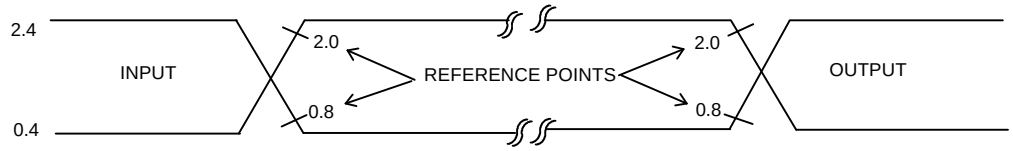
NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} OR T_{BP} DEPENDING UPON THE SELECTED OPERATION MODE.

Figure 12: Data# Polling Timing Diagram



NOTE: THIS TIME INTERVAL SIGNAL CAN BE T_{SE} OR T_{BP} , DEPENDING UPON THE SELECTED OPERATION MODE.

Figure 13: Toggle Bit Timing Diagram



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic “1” and V_{OL} (0.4 V_{TTL}) for a logic “0”. Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 14: AC Input/Output Reference Wav eform

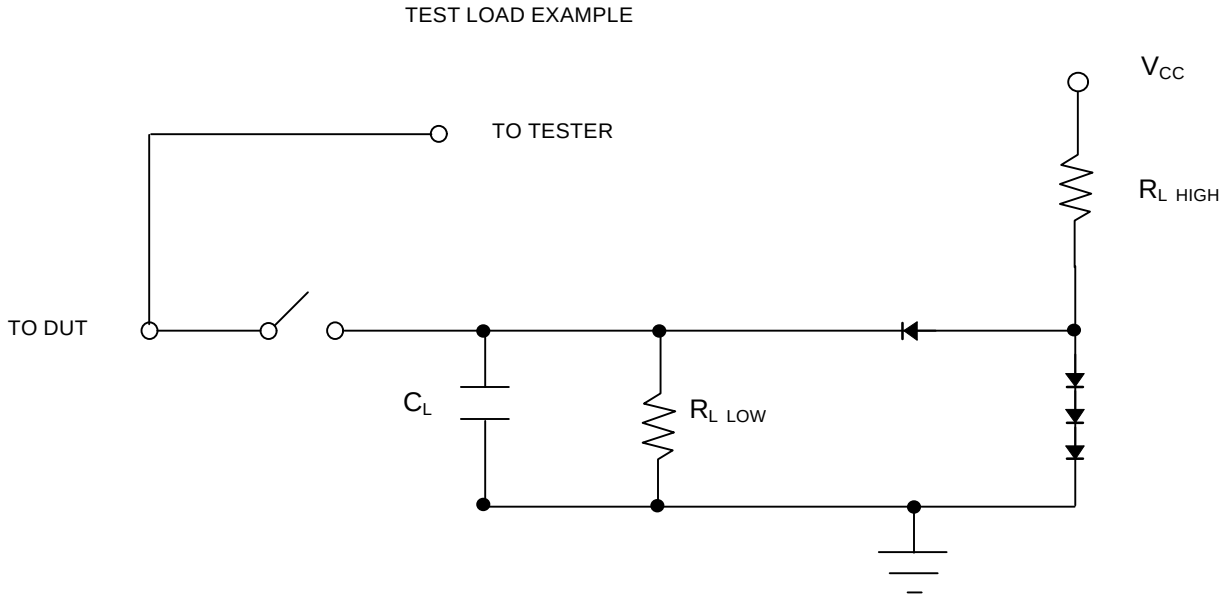


Figure 15: Test Load Example

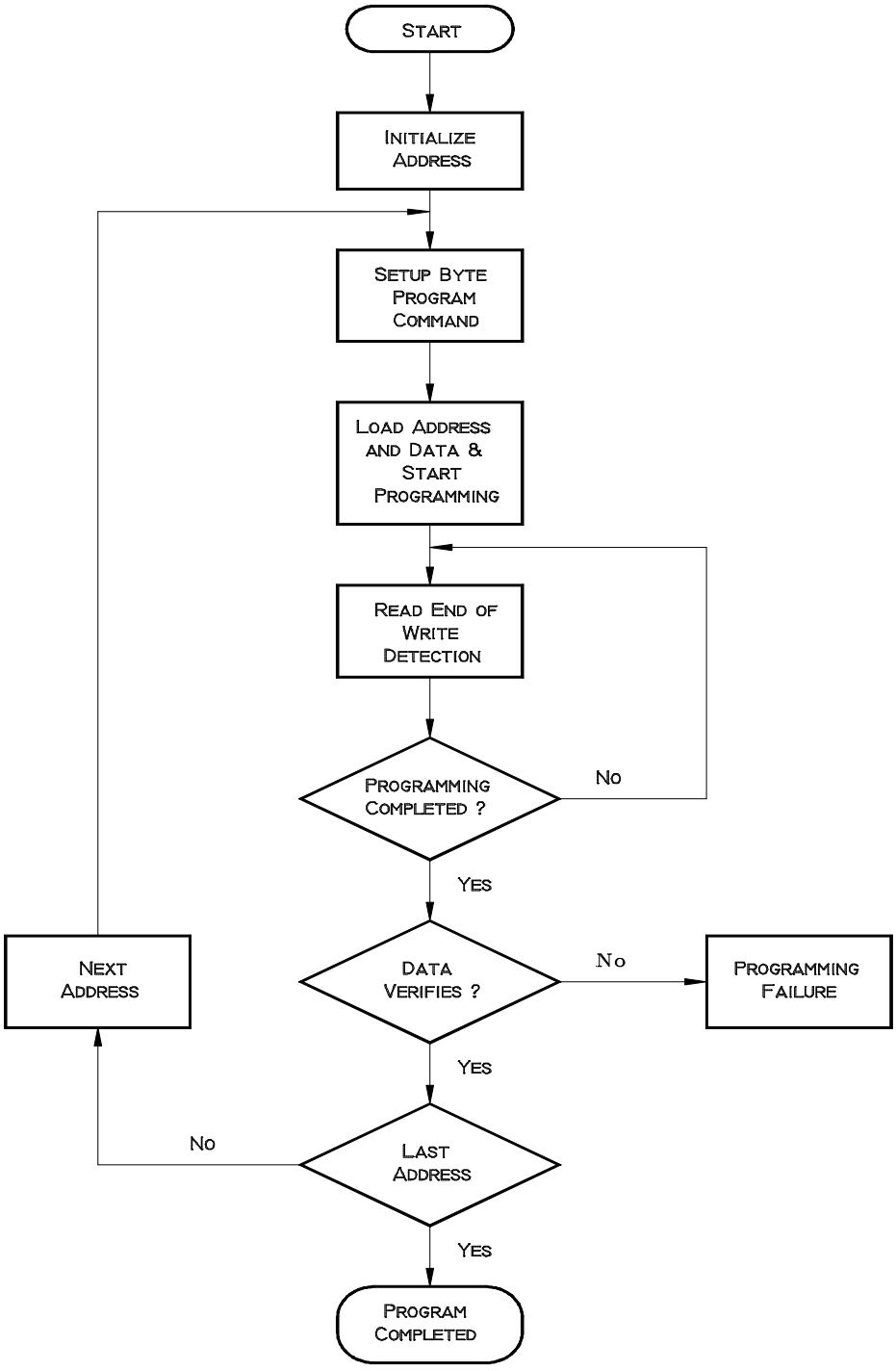


Figure 16: Byte Program Flowchart

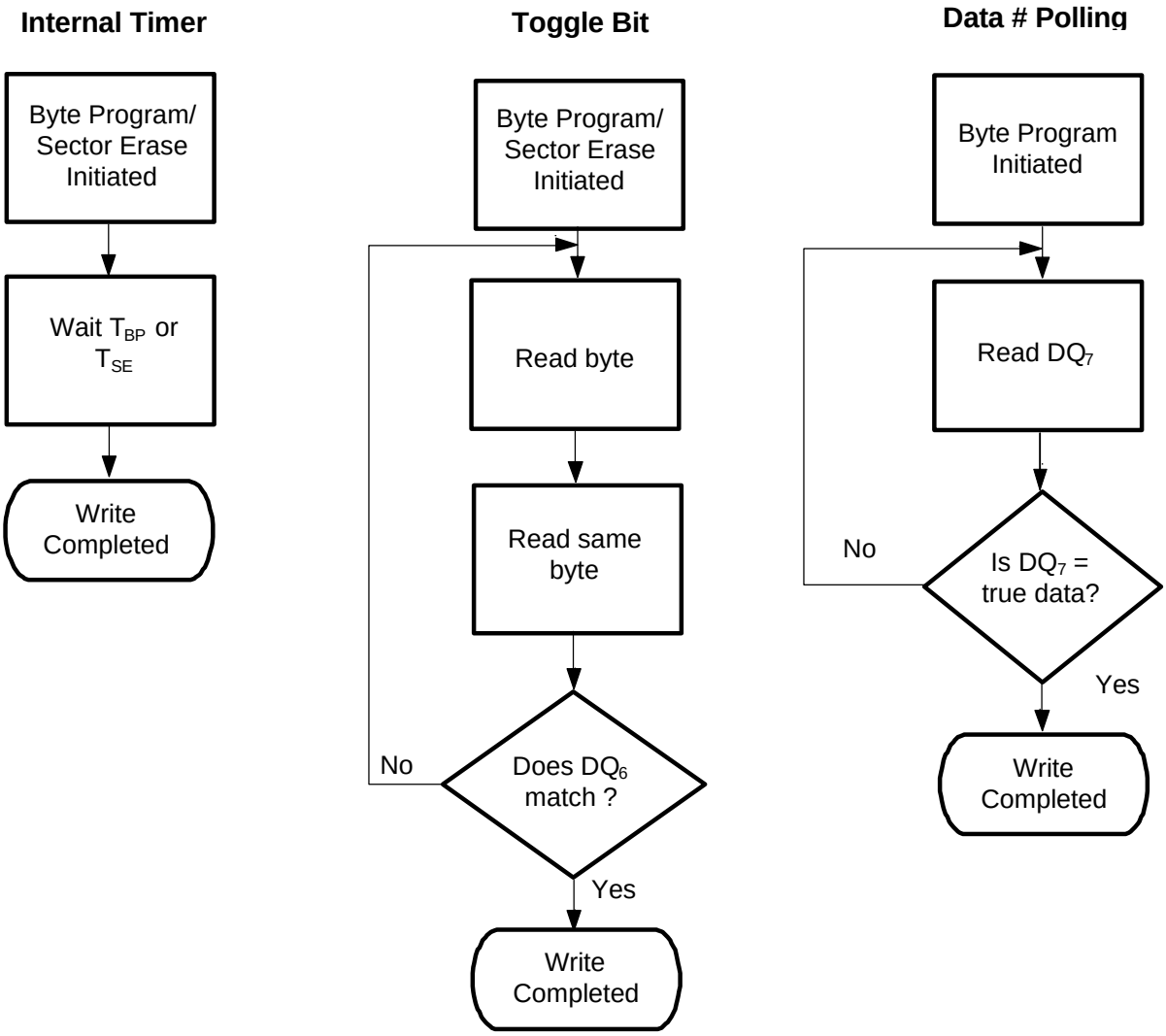


Figure 17: Write Wait Options

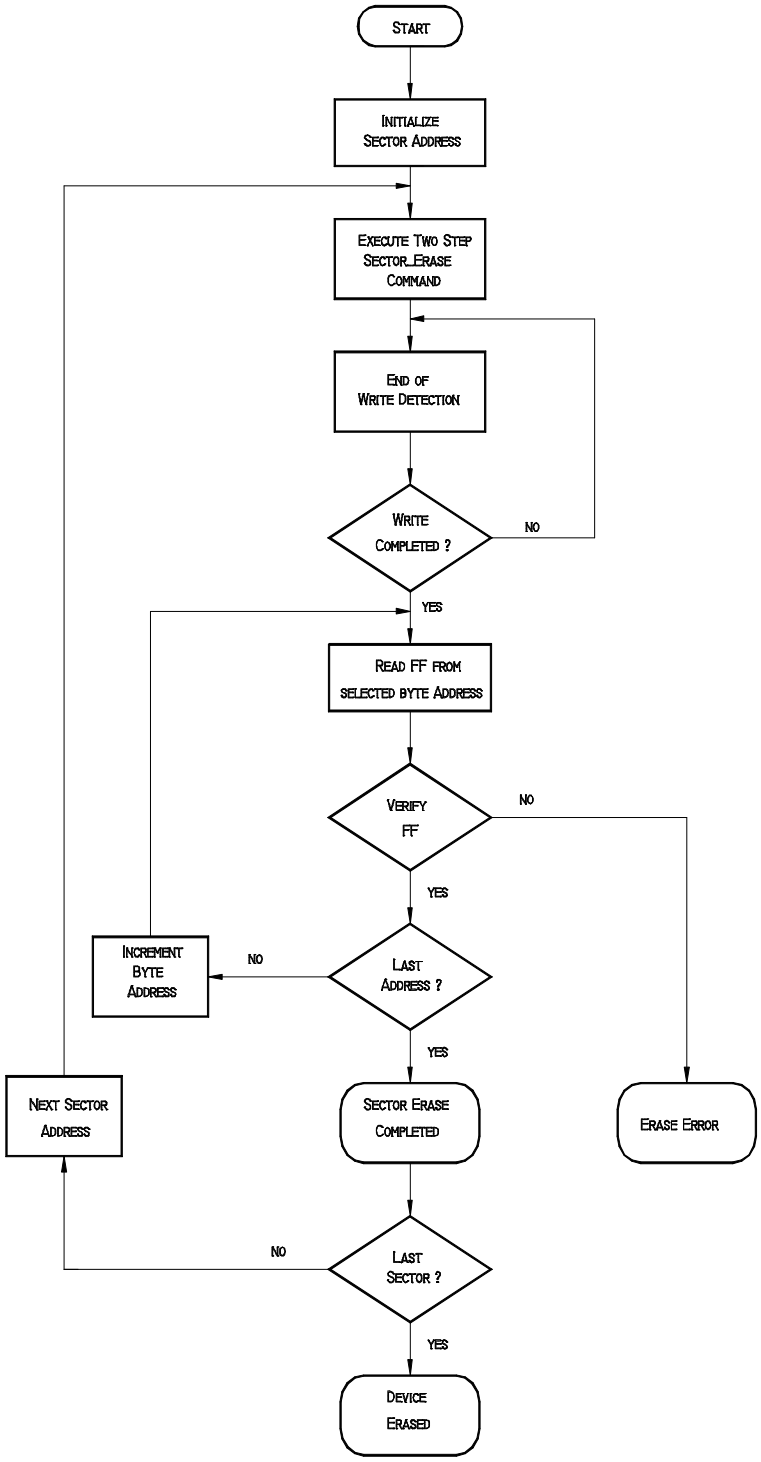


Figure 18: Sector_Erase Flowchart

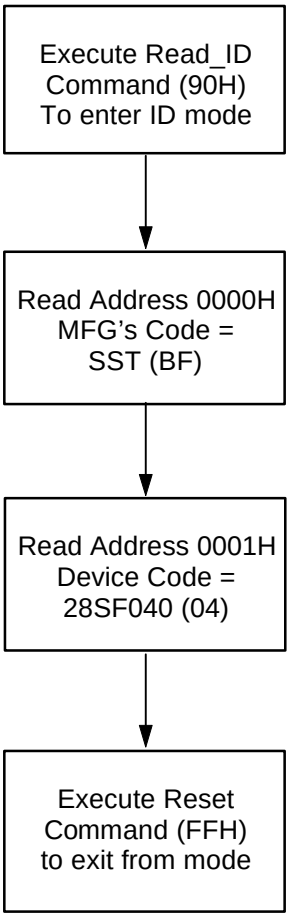


Figure 19: Software Product ID Flow

Product Ordering Information

Device		Speed		Suffix1		Suffix2
SST28SF040	-	XXX	-	XX	-	XX

Package Modifier
I =40 leads
H = 32 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
E = TSOP (die up)
U = Unencapsulated die

Operating Temperature
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
3 = 1000 cycles
4 = 10,000 cycles

Read Access Speed
200 = 200 ns
150 = 150 ns
120 = 120 ns

Valid combinations

SST28SF040-120-4C- EH	SST28SF040-120-4C- EI	SST28SF040-120-4C- NH
SST28SF040-120-4C- PH		
SST28SF040-150-4C- EH	SST28SF040-150-4C- EI	SST28SF040-150-4C- NH
SST28SF040-150-4C- PH		
SST28SF040-200-4C- EH	SST28SF040-200-4C- EI	SST28SF040-200-4C- NH
SST28SF040-200-4C- PH		
SST28SF040-120-3C- EH	SST28SF040-120-3C- EI	SST28SF040-120-3C- NH
SST28SF040-120-3C- PH		
SST28SF040-150-3C- EH	SST28SF040-150-3C- EI	SST28SF040-150-3C- NH
SST28SF040-150-3C- PH		
SST28SF040-200-3C- EH	SST28SF040-200-3C- EI	SST28SF040-200-3C- NH
SST28SF040-200-3C- PH		
SST28SF040-150-4I- EH	SST28SF040-150-4I- EI	SST28SF040-150-4I- NH

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales represent a-tive to confirm availability of valid combinations and to determine availability of new combin ations.